PULSE-WIDTH LIMITED CHIP CLOCK DESIGN

BACKGROUND OF THE INVENTION

Field of the Invention

The invention relates generally to electrical and electronic circuit designs and, more particularly, to a chip clock design that accommodates low frequency or testing environments without sacrificing performance for the normal design environments.

Description of the Related Art

As transistors reduce in size in the newer metal-oxide-silicon field-effect transistor (MOSFET) technologies, T_{OX} (i.e., thickness of the oxide layer) and threshold voltage have also been reducing. When T_{OX} and threshold voltages reduce, there is an increase in leakage currents. Additionally, during chip manufacturing, the transistors are exposed to testing temperatures and voltages. This exposure causes the leakage currents to increase dramatically. Typically, these tests are performed at low frequencies. Low frequency tests, under extreme leakage conditions, make it very difficult to design dynamic logic circuits, because the dynamic logic circuits must be in the evaluation or testing phase for an extended period of time. To insure that the dynamic circuits do not discharge unintentionally due to the excessive exposure to testing environments, it must be considered how much leakage current the dynamic nodes in the dynamic circuits are exposed to. Conventionally, more keeper devices are used to insure functionality under the extreme

test conditions. Using an increased number of keeper devices, however, causes the nominal environment performance to suffer.

Therefore, there is a need for a circuit design that accommodates low frequency or testing environments without sacrificing performance for the normal design environments.

SUMMARY OF THE INVENTION

The present invention provides a method and an apparatus for limiting a pulse width in a chip clock design of a circuit. The circuit receives a clock signal having a clock pulse width. The clock pulse width of the clock signal is detected. It is determined whether the clock pulse width is larger than a maximum clock pulse width. Upon a determination that the clock pulse width is larger than a maximum clock pulse width, the clock pulse width of the clock signal is limited.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIGURE 1 illustrates clock pulses at various frequencies designed to accommodate low frequency or testing environments without sacrificing performance for a normal design environment;

FIGURE 2 illustrates a block diagram showing a general clocking scheme used to accomplish the clock pulses of FIGURE 1;

FIGURE 3 illustrates a schematic diagram showing a preferred embodiment of a pulse-limiting circuit of FIGURE 2;

FIGURE 4 illustrates a schematic diagram showing an alternative embodiment of a pulse-limiting circuit of FIGURE 2;

FIGURE 5 illustrates a timing diagram showing various signals of the alternative embodiment of FIGURE 4 when there is an 8FO4 delay in the input signal;

FIGURE 6 illustrates a timing diagram showing various signals of the alternative embodiment of FIGURE 4 when there is a 10FO4 delay in the input signal;

FIGURE 7 illustrates a timing diagram showing various signals of the alternative embodiment of FIGURE 4 when there is an 11FO4 delay in the input signal;

FIGURE 8 illustrates a timing diagram showing various signals of the alternative embodiment of FIGURE 4 when there is a 15FO4 delay in the input signal;

FIGURE 9 illustrates a timing diagram showing various signals of the alternative embodiment of FIGURE 4 when there is a 16FO4 delay in the input signal;

FIGURE 10 illustrates a timing diagram showing various signals of the alternative embodiment of FIGURE 4 when there is a 30FO4 delay in the input signal;

FIGURE 11 illustrates a timing diagram showing various signals of the alternative embodiment of FIGURE 4 when there is a 31FO4 delay in the input signal; and

FIGURE 12 illustrates a timing diagram showing various signals of the alternative embodiment of FIGURE 4 when there is a 40FO4 delay in the input signal.

DETAILED DESCRIPTION

In the following discussion, numerous specific details are set forth to provide a thorough understanding of the present invention. However, it will be apparent to those skilled in the art that the present invention may be practiced without such specific details. In other instances, well-known elements have been illustrated in schematic or block diagram form in order not to obscure the present invention in unnecessary detail.

It is further noted that, unless indicated otherwise, all functions described herein may be performed in either hardware or software, or some combinations thereof. In a preferred embodiment, however, the functions are performed by a processor such as a computer or an electronic data processor in accordance with code such as computer program code, software, and/or integrated circuits that are coded to perform such functions, unless indicated otherwise.

In the remainder of this description, a processing unit (PU) may be a sole processor of computations in a device. In such a situation, the PU is typically referred to as an MPU (main processing unit). The processing unit may also be one of many processing units that share the computational load according to some methodology or algorithm developed for a given computational device. For the remainder of this description, all references to processors shall use the term MPU whether the MPU is the sole computational element in the device or whether the MPU is sharing the computational element with other MPUs, unless indicated otherwise.

Referring to FIGURE 1 of the drawings, the reference

numeral 100 generally designates clock pulses at various frequencies designed to accommodate low frequency or testing environments without sacrificing performance for a normal design environment. Shown are three example clock pulses 102, 104, and 106. The clock pulses 102 represent clock pulses at normal speed. At normal speed, the clock is unaffected.

The clock pulses 104 represent clock pulses at reduced speed but before a maximum pulse width (not shown) is reached. As the clock frequency is slowed but before the maximum pulse width is reached, the duty factor stays the same as the duty factor provided by a phase-locked loop (PLL) (not shown). Typically, the maximum pulse width varies for different circuits under test. Preferably, the maximum pulse width is determined by the leakage current characteristics of a particular circuit under test and is quantifiable with the number of standard inverter delays. For example, certain circuits under test may have a maximum pulse width equivalent to a pulse width of 15 to 20 standard inverter delays.

The clock pulses 106 represent clock pulses at further reduced speed such that the pulse width reached the maximum pulse width and was further increased. As the frequency is further reduced from the point where the maximum pulse width is reached, the pulse width of the leading clock edge is limited by the present invention. In other words, the clock pulses 106 show that the duty cycle of the clock pulses 106 is altered.

Additional advantages of the present invention include that the present invention enables a chip clock design to have one design point for both high frequency and low frequency applications.

In FIGURE 2, a block diagram shows a general clocking scheme 200 used to accomplish the clock pulses of FIGURE 1. The general clocking scheme 200 includes a phase-locked loop (PLL) 202, a pulse-limiting circuit 204, and optionally an override circuit 206. The PLL 202 is coupled to the pulse-limiting circuit 204 and the optional override circuit 206. The pulse-limiting circuit 204 is coupled to the override circuit 206 and receives a pulse width setting signal. The pulse width setting signal determines the maximum pulse width discussed above in reference to FIGURE 1 and is preferably adjustable. The override circuit 206 receives an override signal to select an output signal from the PLL 202 and the pulse-limiting circuit 204.

Now referring to FIGURE 3, a schematic diagram 300 shows a preferred embodiment of a pulse-limiting circuit 204 of FIGURE 2. The pulse-limiting circuit 300 generally comprises a first p-channel metal-oxide-silicon (PMOS) transistor 302, a second PMOS 304, a first n-channel metal-oxide-silicon (NMOS) transistor 306, a third PMOS 308, a fourth PMOS 310, a second NMOS 312, a third NMOS 314, a first inverter 316, a second inverter 318, a first delay block 320, a second delay block 322, a third delay block 324, a fourth delay block 326, a third inverter 328, and a fourth inverter 330. The delay block 320 includes four AND gates 332, 334, 336, and 338 coupled in series. Similarly, the delay block 322 includes four AND gates 340, 342, 344, and 346 coupled in series. The delay block 324 includes four AND gates 348, 350, 352, and 354 coupled in series. The delay block 326 includes four AND gates 356, 358, 360, and 362 coupled in series.

Although it is shown to include four delay blocks 320,

322, 324, and 326, the pulse-limiting circuit 300 may generally have a plurality of delay blocks to perform the intended function of the present invention. For example, the pulse-limiting circuit 300 may have the first delay block 320 and only one of the remaining three delay blocks. For the sake of convenience, these four delay blocks 320, 322, 324, and 326 are collectively referenced herein as delay blocks 320-326.

The first PMOS 302 is coupled to the supply voltage Vdd and the second PMOS 304 to pull up the source of the second PMOS 304 to Vdd when the output of the third inverter 328 is low. The second PMOS 304 is also coupled to the first NMOS 306 and is configured to be gated by an Nclk_in signal. The first NMOS 306 is coupled to ground and is configured to be gated by the Nclk_in signal. The output of the first inverter 316 is coupled to the input of the second inverter 318, the output of which is also coupled to the input of the first inverter 316. Node nfb is shown as the output of the first inverter 316, whereas node fb is shown as the output of the second inverter 318.

The third PMOS 308 is coupled between Vdd and the source terminal of the fourth PMOS 310 and is gated by node fb. Thus, when node fb is low, the third PMOS 308 pulls up the source of the fourth PMOS 310 to Vdd. The fourth PMOS 310 is also coupled to both the drain terminals of the second NMOS 312 and the third NMOS 314 and is gated by Nclk_in. The second NMOS 312 and the third NMOS 314 are coupled in parallel between the drain terminal of the fourth PMOS 310 and ground. The second PMOS 304, the first NMOS 306, the fourth PMOS 310, and the second NMOS 312 are all gated by Nclk_in. Both the third PMOS

308 and the third NMOS 314 are gated by node fb.

The first delay block 320 is coupled to Vdd and the drains of the second NMOS 312 and the third NMOS 314. Node a0 is shown to indicate one input to the first delay block 320. Specifically, the NAND gate 332 is coupled to both Vdd and node a0. Therefore, the NAND gate 332 functions as an inverter. The output of the first delay block 320 is shown as node a5. The NAND gate 340 is coupled to both nodes a0 and a5. Similarly, the output of the second delay block 322 is shown as node a10. The NAND gate 348 is coupled to both nodes a0 and a10. Likewise, the output of the third delay block 324 is shown as node a15. The NAND gate 356 is coupled to both nodes a0 and a15. The output of the fourth delay block 326 is shown as node a20, which is coupled to the input of the third inverter 328. The fourth inverter 330 is coupled to node a0 and generates an inverted signal of node a0 as Nclk_out.

The pulse-limiting circuit 300 assumes the down pulse is the one that is to be limited. A similar pulse-limiting circuit for limiting the up pulse may be apparently derived from the pulse-limiting circuit 300. Initially, the "nclk_in" signal is high. Nodes a0-a20 are low, and the feedback signal "fb" is low. As nclk_in goes to low, node a0 goes to high. After some delay, node a5 goes to high. Subsequently, nodes a10, a15, and a20 go to high sequentially. When node a20 goes high, node na20 goes low, turning on the first PMOS 302. This in turn drives node fb high. When node fb goes high, node a0 returns low again, forcing the output "nclk_out" to go high. The down pulse of the "nclk_out" signal is limited to the loop delay of the circuit. Since node a0 is passed to multiple points in the delay chain consisting of the delay blocks, the

chain resets very quickly, causing node a20 to go low again, to get ready for the next input clock cycle. The node fb is designed to reset the nclk_out high but not low. Only the input clock "nclk_in" can reset the nclk_out low.

In the case where the input clock "nclk_in" has a pulse width shorter than the loop delay, the nclk_in is passed directly to nclk_out via the input devices, since node fb never goes high. This is because the loop resets much faster than its sets, and thus the transition of node a20 is blocked.

It is noted that there are many different ways to implement each delay block without departing from the true spirit of the invention. Also note that NAND gates in these four delay blocks are replaceable with an inverter or other forms of delay elements.

As briefly mentioned above, PMOS and NMOS stand for p-channel and n-channel metal-oxide-silicon transistors, respectively. MOS transistors are field effect transistors (FETs) and generally have gate, source, and drain terminals. Detailed explanation of orientations and/or connections of PMOS and NMOS transistors with respect to these terminals are well known in the art from the symbols used to represent these transistors and thus may be omitted herein in order not to unnecessarily complicate the description. Since PMOS and NMOS transistors described herein primarily function as digital switches, the present invention should be considered to cover different implementations using such switches in place of the PMOS and NMOS transistors without departing from the true spirit of the present invention.

Now referring to FIGURE 4, a schematic diagram 400 shows an alternative embodiment of a pulse-limiting circuit of

FIGURE 2. The pulse-limiting circuit 400 comprises an input clock 402, a first transport delay 404, a second transport delay 406, a first NOT logic 408, a first one-shot logic 410, a second one-shot logic 412, a third one-shot logic 414, a first D flip-flop (DFF) 416, a second D flip-flop (DFF) 418, a fourth one-shot logic 420, a first AND logic 422, a second AND logic 424, a third AND logic 426, a first OR logic 428, a second NOT logic 430, a second OR logic 432, a third NOT logic 434, a first NAND logic 436, and a second NAND logic 438.

The input clock 402 is coupled to the first transport delay 404, a first NOT logic 408, a first DFF 416, a second DFF 418, and a fourth one-shot logic 420 to provide the input clock pulse of the input clock 402. The first transport delay 404 generates a Cd1 signal, which is a delayed signal of the input clock pulse by a delay amount of 7.5FO4. This delay amount refers to the delay of 7.5 inverters with four inverters like itself as output loads. For example, 1FO4 represents the delay of one inverter with fan-out of four. FO is a relative unit of delay, independent of technology and may be replaced with other measures of delay.

The first transport delay 404 is coupled to the second transport delay 406 and the first one-shot logic 410 to provide the Cd1 signal. The first one-shot logic 410 generates a Cdp signal by creating a pulse from a single edge of the Cd1 signal. The second transport delay 406 is coupled to the second one-shot logic 412 to provide the Cd1 signal. The second one-shot logic 412 generates a same Cd1p signal. The first NOT logic 408 is coupled to the third one-shot logic 414 to provide a Cb signal. The third one-shot logic 414 also generates a Cbp signal.

The first DFF 416 is coupled to the first one-shot 410 for receiving the Cdp signal from the first one-shot logic 410 as a clock input. The first DFF 416 is also coupled to the input clock 402 for receiving the input signal as a data input. Similarly, the second DFF 418 is coupled to the second one-shot logic 412 for receiving the Cd1p signal as a clock input and is also coupled to the input clock 402 for receiving the input signal as a data input. The first DFF 416 generates an S1 signal as a data output and an S1b signal as an inverted data output. The second DFF 418 generates an S2 signal as a data output and an S2b signal as an inverted data output.

The fourth one-shot logic 420 generates a SET signal. The first AND logic 422 is coupled to the first DFF 416, the second DFF 418, and the second one-shot logic 412 for receiving the S1, S2, and Cd1p signals. The first AND logic 422 generates a LIMIT signal. The second AND logic 424 is coupled to the first DFF 416 for receiving the S1b signal and is also coupled to the third one-shot logic 414 for receiving the Cbp signal. The third AND logic 426 is coupled to the second DFF 418 for receiving the S2b signal and is coupled to the third one-shot logic 414 for receiving the Cbp signal. The second NOT logic 430 is coupled to the fourth one-shot logic 420 for receiving the SET signal and generates a SETB signal. The first OR logic 428 is coupled to the second AND logic 424 and to the third AND logic 426 for receiving a NOLIMIT1 signal and a NOLIMIT2 signal, respectively. The first OR logic 428 generates a NOLIMIT signal.

The second OR logic 432 is coupled to the first AND logic 422 for receiving the LIMIT signal and is coupled to the first OR logic 428 for receiving the NOLIMIT signal. The second OR

logic 432 generates a RESET signal. The third NOT logic 434 is coupled to the second OR logic 432 for receiving the RESET signal and generates a RESETB signal. The first NAND logic 436 is coupled to the second NOT logic 430 for receiving the SETB signal. The second NAND logic 438 is coupled to the third NOT logic 434 for receiving the RESETB signal. The first NAND logic 436 and the second NAND logic 438 are coupled to each other such that the output of one logic is fed back to the input of the other logic. The first NAND logic 436 and the second NAND logic 438 generate outputs Q and Qb, respectively. Note that the output Q of FIGURE 4 corresponds to the output of the pulse-limiting circuit 204 of FIGURE 2.

There are two delays, one at 7.5FO4 and the other at 15FO4. Pulsed-latches latch the value of the clock at these two delays. If they are both high, pulse-width limiting should be used. This corresponds to 30FO4 and longer cycle times. There is duty cycle sensitivity at 7.5FO4, 15FO4, and 30FO4, which exact cycle times should be avoided.

Now referring to FIGURES 5 through 12, timing diagrams 500, 600, 700, 800, 900, 1000, 1100, and 1200 are various signals of the alternative embodiment of FIGURE 4 when there are various delays in the input signal. The delays in the input signal for FIGURES 5 through 12 are 8FO4, 10FO4, 11FO4, 15FO4, 16FO4, 30FO4, 31FO4, and 40FO4, respectively. Since the pulse-limiting circuit 400 is supposed to affect only signals with 30FO4 and longer cycle times, the output Q is shown to be limited only in FIGURES 11 and 12.

It will be understood from the foregoing description that various modifications and changes may be made in the preferred embodiment of the present invention without departing from its

true spirit. This description is intended for purposes of illustration only and should not be construed in a limiting sense. The scope of this invention should be limited only by the language of the following claims.